JSPM's
RAJARSHI SHAHU COLLEGE OF ENGINEERING
TATHAWADE, PUNE-33
(An Autonomous Institute Affiliated to Savitribai Phule Pune University, Pune)
Department of Electronics & Telecommunication

Date: 27/01/2025

Report

Seminar on "Digital Circuit Design using Deldsim"

(Under IEI Student's Chapter on 27thJanuary 2025)

Class : FY Electronics and Telecommunication Engineering

Name of Session : Digital Circuit Design using Deldsim

Date & Day :Mon, 27th JAN 2025

Total No. of students : 85

Name of College : JSPM's RSCOE, Pune

TYBTech E&TC students as **resource person**

1. Deven Pujari
2. Nikhil Jadhav
3. Shounak Sanpurkar
4. Sahil Arankalle
5. Loukik Sancheti

PO Mapped:

PO1. Engineering knowledge:

Graduates can apply the knowledge of mathematics, science, engineering fundamentals and an engineering specialization to E & TC Engineering related problems.

PO3.Design/development of Solutions:

Design solutions for complex engineering problems and design system components or processes that meet t h e specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

PO4.Conduct Investigations of Complex Problems:

Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

PO5.Modern Tool usage:

Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations.

PO12. Life-long learning:

An ability to engage in independent and life-long learning in the broadest context of Technological change.

Inauguration of the session was done by Dr.C.V.Rane, Faculty Adviser of IEI Student's Chapter. The Session began with brief introduction of the Deldsim software by TY student Sahil Arankalle.

The session was conducted by Third Year students of Entc department of RSCOE. The target audiences were the first year E&TC students. It was specially organized so that FY students can participate in the innovision-2025 event 'Circuitrix'

Workshop Activity: Digital Circuit Design Using Deldsim

Activity 1: Basic Logic Gates

Understanding fundamental logic gates (AND, OR, NOT, NAND, NOR, XOR, XNOR).
Studying truth tables and working principles.

Activity 2: Implementing Basic Gates in Deldsim

- Introduction to Deldsim software.
- Steps to design and simulate basic gates.

- Observing output behavior using truth tables.

Activity 3: Circuit Design and Optimization Using K-Map

- Understanding Karnaugh Map (K-Map) for Boolean simplification.
- Reducing complex Boolean expressions using K-Map.
- Designing optimized digital circuits using simplified expressions.

Followed by a query session between the speaker students and FY students. Students asked various queries to the Senior student speakers who responded with suitable solutions and information.

The whole session is organized by students of ENTC department of the college who are also the part IEI student's chapter.

Third year E&TC students interacting with the FYBTech E&TC students

Dr. C.V. Rane	Dr. C.V. Rane	Dr. S.C. Wagaj
Event Coordinator	**Faculty Advisor**	**Head of E&TC Dept.**
IEI Student's Chapter		